REMARKS

The Office Action of January 28, 2004 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

The specification, claims and drawings were objected to for various informalities. These informalities are addressed in the present amendment.

Claims 1-9 were rejected as being anticipated by the Admitted Prior Art (APA) as described in the present specification, or unpatentable over APA in view of Dias. Claims 1, 3 and 6-9 have been cancelled and new claims 10-13 added. Reconsideration is respectfully requested.

New claims 10, 11 and 12 are respectively directed to a tester, an integrated circuit with test features, and a method of testing logic circuitry in an integrated circuit.

The tester of claim 10 includes a programmable test vector generator for generating test vectors for the logic circuitry. As described in APA, conventional testers include: 1) *memory* (not logic) testers including a rudimentary programmable test vector generator; and 2) logic testers including a test vector memory for storing pre-computed test vectors. Additionally, BIST conventionally provides for integrated circuits having a *non-programmable* test vector generator. There is no teaching or suggestion in APA or in the cited references of the tester of claim 10 including a programmable test vector generator for generating test vectors for the logic circuitry.

The IC of claim 11 includes means for receiving from an external tester test vectors for the logic circuitry, and means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester. As described in APA, conventional ICs include: 1) ICs including means for receiving from an external tester test vectors for the logic circuitry, but *not including* means for receiving from the

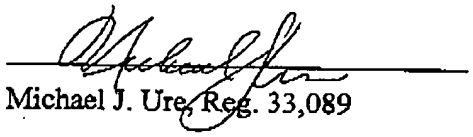
logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester; and 2) ICs including means for means for receiving from the logic circuitry test results in response to test vectors, for producing a compact representation of test results; and for outputting said compact representation to the external tester, but *not including* means for receiving from an external tester test vectors for the logic circuitry. There is no teaching or suggestion in APA or in the cited references of the IC of claim 11 including both means for receiving from an external tester test vectors for the logic circuitry, and means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

The testing method of claim 12 relates to features of both the tester of claim 10 and the integrated circuit of claim 11 and is believed to be patentable for similar reasons.

Accordingly, claims 10-12 are believed to patentably define over the cited references.

Dependent claims 2, 4, 5 and 13 are also believed to add novel and patentable subject matter to their respective independent claims. Withdrawal of the rejection and allowance of claims 2, 4, 5 and 10-13 is respectfully requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: March 9, 2004